

CLAIMS

What is claimed is:

1 1. A switch matrix circuit comprising:
2 a plurality of switches organized in a row and column configuration; and
3 a current sensing circuit coupled to the plurality of switches, the current sensing
4 circuit including a transistor and at least one resistor per column of the plurality of switches,
5 wherein current amplified by the transistor and converted by the at least one resistor in a
6 column is sensed as a logic level indicative of a switch status within the column for a
7 selected row.

1 2. The switch matrix circuit of claim 1 wherein the transistor further comprises a bipolar
2 junction transistor.

1 3. The switch matrix circuit of claim 1 wherein the row and column configuration
2 further comprises an off-diagonal configuration having one switch per row and column
3 intersection in all but one intersection per row.

1 4. The switch matrix circuit of claim 3 wherein each intersection lacking a switch
2 lies in a different column within each row.

1 5. The switch matrix circuit of claim 4 wherein a single scan line supports providing
2 a row input signal or reading a column output signal for one row and one column within the
3 off-diagonal configuration.

1 6. The switch matrix circuit of claim 1 wherein a processor senses the switch status.

1 7. A circuit for more efficient switch selection sensing, the circuit comprising:
2 a switch matrix comprising a plurality of switches organized as a plurality of rows
3 and columns;
4 a current sensing circuit coupled to the switch matrix; and
5 a processor coupled to the switch matrix and the current sensing circuit by a plurality
6 of scan lines, wherein selection of a row by a scan line returns column current levels from
7 the current sensing circuit to detect if a switch at a row and column intersection of the switch
8 matrix has been selected.

1 8. The circuit of claim 7 wherein the plurality of scan lines further comprise a
2 plurality of bi-directional scan lines wherein a single scan line provides both row selection
3 and column sensing capabilities.

1 9. The circuit of claim 8 wherein the organization of the plurality of switches further
2 comprise an off-diagonal organization to support the bi-directional scan lines.

1 10. The circuit of claim 7 wherein the current sensing circuit further comprises a
2 transistor and resistor circuit for each column in the switch matrix.

1 11. The circuit of claim 10 wherein the column current levels indicate when the
2 transistor is turned on and current passes through the resistor.

1 12. The circuit of claim 10 wherein the transistor further comprises a bipolar
2 junction transistor.

1 13. A method for sensing switch status, the method comprising:
2 coupling a current sensing circuit to a switch matrix having a plurality of switches in
3 a row and column configuration; and
4 utilizing a processor to detect switch status within the switch matrix based on current
5 signals in the current sensing circuit.

1 14. The method of claim 13 further comprising forming the current sensing circuit as
2 a transistor and at least one resistor per column of the plurality of switches.

1 15. The method of claim 14 wherein utilizing a processor to detect switch status
2 further comprises detecting current amplified by the transistor and converted by the at least
3 one resistor in a column as a logic level indicative of the switch status within the column for
4 a selected row.

1 16. The method of claim 15 wherein utilizing a processor further comprises utilizing
2 a plurality of bi-directional scan lines, wherein a single scan line provides both row selection
3 and column sensing capabilities.

1 17. The method of claim 16 further comprising organizing the plurality of switches
2 as an off-diagonal organization to support the bi-directional scan lines.

1 18. The method of claim 14 further comprising utilizing a bipolar junction transistor
2 as the transistor.

1 19. A switch matrix circuit comprising:
2 a plurality of switches organized in a row and column off-diagonal configuration
3 having one switch per row and column intersection in all but one intersection per row; and

4 a plurality of scan lines comprising a plurality of bi-directional scan lines, wherein a
5 single scan line provides both row selection and column sensing capabilities for switch
6 selection identification.

1 20. The switch matrix of claim 19 wherein the one intersection per row lacking a
2 switch lies in a different column within each row.
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1 21. The switch matrix of claim 19 wherein an analog to digital converter senses a
2 switch status.
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1 22. The switch matrix of claim 19 further comprising a diode and resistor circuit for
2 each scan line.
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1 23. A circuit for more efficient switch selection sensing, the circuit comprising:
2 a switch matrix including
3 a plurality of switches organized as a plurality of rows and columns; and
4 a plurality of resistors, each of the resistors electrically coupled in series with an
5 associated one of the plurality of switches;
6 a voltage threshold sensing circuit coupled to the switch matrix by a plurality of scan
7 lines; and

8 a processor coupled to the voltage threshold sensing circuit by a signal bus, wherein
9 selection of a row by a scan line returns column voltage levels from the switch matrix to
10 detect if a switch at a row and column intersection of the switch matrix has been selected.

1 24. The circuit of claim 22 wherein the voltage threshold sensing circuit converts the
2 column voltage levels to logic states.

1 25. The circuit of claim 24 wherein the voltage threshold sensing circuit includes an
2 analog to digital converter.

1 26. The circuit of claim 24 wherein the voltage threshold sensing circuit includes a
2 voltage level converter including a transistor.